What is claimed is:

1. A method for fabricating a MOS device having a gate width of less than 0.3 micron that comprises the steps of:

(a) forming an interfacial layer on a semiconductor substrate of a first conductivity type;

(b) forming a high dielectric constant layer on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) depositing a layer of electrically conductive material on the high dielectric constant layer;

(d) selectively removing portions of the layer of electrically conductive material to form a gate electrode and to expose portions of the high dielectric constant layer;

(e) implanting impurity ions through the exposed portions of the high dielectric constant layer into the substrate to form source and drain regions of a second conductivity type;

(f) forming first spacers that are adjacent the gate electrode and cover portions of the source and drain regions of the second conductivity type;

(g) removing the exposed portions of the high dielectric constant layer;

(h) implanting a second dose of impurity ions into the source and drain regions;

(i) depositing a layer of insulator material over the surface of the device;

(j) optionally, planarizing the surface of the insulator material;

(k) removing portions of the insulator material to form contact holes in the insulator material that are in communication with the source and drain regions; and

(l) filling the contact holes with contact material.

2. The method of claim 1 comprising the step of densifying the high dielectric constant layer.

3. The method of claim 1 wherein the electrically conductive material comprises metal that is selected from the group consisting of TiN, W, Ta, Mo and multilayers thereof.

4. The method of claim 1 wherein the electrically conductive material comprises doped polysilicon.

5. The method of claim 4 further comprising the step of forming a barrier layer between the electrically conductive material and the high dielectric constant layer.

6. The method of claim 1 further comprising the step of forming second spacers that are adjacent the first spacers and cover portions of the source and drain regions following step (g) and before step (h).

7. The method of claim 1 further comprising the step of forming a silicide layer on the source and drain regions following step (h).

8. The method of claim 7 wherein forming the silicide layer comprises the steps of:

depositing a layer of metal over the at least the source and drain regions;

heating the layer of metal to cause the metal to react with the silicon on the surface of the source and drain regions to form metal silicide layers in the source and drain regions; and

removing unreacted metal from the layer of metal.

9. The method of claim 7 wherein forming the silicide layer comprises selectively depositing silicide over the source and drain regions.

10. The method of claim 1 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

11. The method of claim 1 wherein the interfacial layer comprises silicon oxide, silicon nitride, or silicon oxynitride.

12. The method of claim 1 wherein step (h) comprises introducing a light dosage of impurities to form lightly doped source and drain regions.

13. The method of claim 1 wherein the high dielectric constant material is Ta_2O_5.

14. The method of claim 1 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6.

15. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

16. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

17. The method of claim 1 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

18. The method of claim 1 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

19. The method of claim 1 wherein the substrate comprises silicon.

20. The method of claim 1 wherein the first spacers comprise an oxide or nitride material.

21. The method of claim 1 wherein step (i) comprises depositing a conformal layer of insulator material and (j) planarizes the surface of the insulator material by chemical mechanical planarization.

22. An MOS transistor formed on a semiconductor substrate of a first conductivity type comprising:

(a) an interfacial layer formed on the substrate;

(b) a high dielectric constant layer covering the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate;

(c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer;

(d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface;

(e) a source and drain regions of a second conductivity type; and

(f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

23. The MOS transistor of claim 22 comprising:

(g) an insulator layer covering the device and defining a first contact hole that is filled with a first contact material and a second contact hole that are filled with a second contact material, wherein the insulator layer has a substantially planar surface.

24. The MOS transistor of claim 22 wherein the gate electrode is formed from a metal that is selected from the group consisting of TiN, W, Ta, MO and multilayers thereof.

25. The MOS transistor claim 22 wherein the gate electrode comprises doped polysilicon.

26. The MOS transistor of claim 25 comprising a barrier layer between the gate electrode and the high dielectric constant layer.

27. The MOS transistor of claim 22 comprising a pair of second spacers that are adjacent to the first spacers and formed on the lightly doped regions.

28. The MOS transistor of claim 22 comprising a silicide layer on the source and drain regions.

29. The MOS transistor of claim 22 wherein the high dielectric constant material layer has a thickness that ranges from about 4 nm to 12 nm.

30. The MOS transistor of claim 22 wherein the high dielectric constant material is Ta_2O_5.

31. The MOS transistor of claim 22 wherein the high dielectric constant material is $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from 0 to 0.6.

32. The MOS transistor of claim 22 herein the high dielectric constant material is a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r preferably ranges from about 0.9 to 1.

33. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to 1.

34. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to 1.

35. The MOS transistor of claim 22 wherein the high dielectric constant material is a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to 1.

36. The MOS transistor of claim 22 wherein the substrate comprises silicon.

37. The MOS transistor of claim 22 wherein the first spacers comprise an oxide or nitride material.